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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,151	09/22/2003	Vishnu K. Agarwal	M4065.0195/P195-B	5782
24998	7590	08/10/2006	EXAMINER	
DICKSTEIN SHAPIRO LLP 1825 EYE STREET NW Washington, DC 20006-5403			PHAM, HOAI V	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/665,151

Applicant(s)

AGARWAL ET AL.

Examiner

Hoai v. Pham

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 11 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-12, 14, 15, 23, 28, 39, 44, 77-81, 84 and 85 is/are pending in the application.
- 4a) Of the above claim(s) 4, 7, 12, 14 and 15 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5, 6, 8, 23, 28, 78-81, 84 and 85 is/are rejected.
- 7) ☒ Claim(s) 9-11 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Objections*

1. Claim 79 is objected to because of the following informalities:

Line 4, change "at lest" to --at least--.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5, 6, 8, 23, 28, 78, 81 and 84-85 are rejected under 35 U.S.C. 102(e) as being anticipated by Hieke [U.S. Pat. 6,188,095] newly cited.

With respect to claim 1, Hieke (figs. 3-4, cols. 1-3) discloses a monolithic semiconductor device comprising:

a semiconductor substrate (silicon wafer) (col. 2, lines 53-60);

a plurality of microstructures (7) formed over the substrate, wherein the microstructures are stud capacitor (col. 2, lines 24-26); and

a brace (8, 9) transversely extending between lateral sides of at least two of the microstructures (7); and

a vertical space between said brace and said semiconductor substrate.

With respect to claim 2, Hieke discloses that the brace (8, 9) interconnects substantially all of the microstructures (7) (see fig. 4).

With respect to claim 3, Hieke discloses that the brace (8, 9) is located substantially near upper ends of the microstructures (7) (see fig. 4).

With respect to claim 5, Hieke discloses that the brace (8, 9) comprises a microbridge structure extending above the substrate and between two or more of the microstructures (7) (see fig. 4).

With respect to claim 6, Hieke discloses that the microstructures (7) each comprise a conductor material portion standing upright over the substrate, and wherein the brace (8, 9) interconnects the conductor material portion of two or more of the microstructures (7) (see fig. 4).

With respect to claim 8, Hieke discloses that the microstructures (7) comprise generally solid cylindrical shapes and the brace comprises a microbridge structure (fig. 4).

With respect to claim 23, Hieke (figs. 3-4, cols. 1-3) discloses a semiconductor storage capacitor comprising:

- a semiconductor substrate (silicon wafer) (col. 2, lines 53-60);

- a plurality of capacitor storage node microstructures (7) formed over the substrate; and

- a brace (8, 9) transversely extending between lateral sides of at least two of the microstructures (7), wherein the microstructures comprise generally solid cylindrical shapes and the brace comprises a microbridge structure, and wherein there is a vertical space between said brace and said semiconductor substrate.

With respect to claim 28, Hieke (figs. 3-4, cols. 1-3) discloses a semiconductor storage capacitor comprising:

- a semiconductor substrate (silicon wafer) (col. 2, lines 53-60);

- capacitor storage node microstructures (7) formed over the substrate; and

- a brace (8, 9) transversely extending between lateral sides of at least two of the microstructures, wherein the microstructures comprise stud capacitors, and wherein there is a vertical space between said brace and said semiconductor substrate.

With respect to claim 78, Hieke (figs. 3-4, cols. 1-3) discloses a support structure on a semiconductor device comprising:

a plurality of braces (8, 9) transversely extending between lateral sides of microstructure (7) formed over a semiconductor substrate (silicon wafer) (col. 2, lines 53-60), said microstructure (7) comprising a generally solid cylindrical shape, wherein said plurality of braces (8, 9) comprise a support structure for said microstructure (7); and a vertical space between the plurality of braces (8, 9) and the semiconductor substrate.

With respect to claim 81, Hieke (figs. 3-4, cols. 1-3) discloses a semiconductor support structure, comprising:

- a semiconductor substrate (silicon wafer) (col. 2, lines 53-60);
- a plurality of microstructures (7) formed over the substrate ; and
- a plurality of braces (8, 9) transversely extending between lateral sides of at least two of said plurality of microstructures (7), wherein said plurality of brace (8, 9) comprises a lattice support structure wherein said plurality of brace (8, 9) intersect at said microstructures (7), and wherein there is a vertical space between the support structure and the semiconductor substrate.

With respect to claim 84, Hieke (figs. 3-4, cols. 1-3) discloses a semiconductor storage capacitor comprising:

- a semiconductor substrate (silicon wafer) (col. 2, lines 53-60);
- a plurality of capacitor storage node microstructures (7) formed over the substrate, said microstructures (7) having vertical surfaces;

a brace (8, 9) transversely extending between the vertical surfaces of at least two of the microstructures (7), said brace being located substantially near the upper ends of said vertical surfaces of said microstructures; and

a vertical space between said brace and said substrate.

With respect to claim 85, Hieke (figs. 3-4, cols. 1-3) discloses semiconductor storage capacitor, comprising:

a semiconductor substrate (silicon wafer) (col. 2, lines 53-60);

capacitor storage node microstructures (7) formed over the substrate, said microstructures having vertical surfaces; and

a plurality of braces (8, 9) transversely extending between the vertical surfaces of at least two of the microstructures, said plurality of braces being located substantially near the upper ends of said vertical surfaces of said microstructures (7), and wherein there is a vertical space between said plurality of braces and said semiconductor substrate.

4. Claims 78 is rejected under 35 U.S.C. 102(e) as being anticipated by Hirose [U.S. Pat. 6,097,097] newly cited.

Hirose (fig. 1A, col. 4) discloses a support structure on a semiconductor device comprising:

a plurality of braces (1) transversely extending between lateral sides of microstructure (3) formed over a semiconductor substrate (2), said microstructure (3) comprising a generally solid cylindrical shape, wherein said plurality of braces (1)

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comprise a support structure for said microstructure (3); and a vertical space (10) between the plurality of braces (1) and the semiconductor substrate.

5. Claims 79 and 80 are rejected under 35 U.S.C. 102(e) as being anticipated by Al-Shareef et al. [U.S. Pat. 6,351,005] newly cited.

With respect to claim 79, Al-Shareef et al. (fig. 8b, cols. 4-10) discloses a brace for a semiconductor device comprising:

at least one brace (20) transversely extending between lateral sides of at least two microstructures (30) on a semiconductor substrate (10), said at least two microstructures (30) comprising stud capacitors, wherein said at least two microstructures (30) are supported only by said at least one brace (20), wherein said at least one brace comprises one material layer.

With respect to claim 80, Al-Shareef et al. (fig. 8b, cols. 4-10) discloses an in-process semiconductor device comprising:

a semiconductor substrate (10);

at least two microstructures (30) formed over the substrate (10), said at least two microstructures (30) comprising generally solid cylindrical shapes; and

at least one brace (20) transversely extending between lateral sides of at least two microstructures (30), wherein said at least two microstructures (30) are supported only by said at least one brace (20), and wherein said at least one brace comprises a single material layer.

***Allowable Subject Matter***

6. Claims 39, 44, and 77 are allowed.
7. Claim 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Response to Arguments***

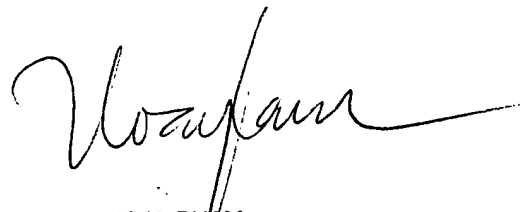
8. Applicant's arguments with respect to claims 1-3, 5-6, 8, 23, 28, 78-81 and 84-85 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.
10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



HOAI PHAM  
PRIMARY EXAMINER